REMARKS/ARGUMENTS

Claims 1-20 stand rejected in the outstanding Official Action. Claims 2 and 12 have been cancelled without prejudice and claims 1, 3, 11 and 13 amended. Therefore, claims 1, 3-11 and 13-20 are the only claims remaining in this application.

The Examiner's acknowledgment of Applicant's claim for foreign priority and receipt of the certified copies of the priority documents is very much appreciated. Additionally, the Examiner's consideration of the prior art previously submitted with Applicant's Information Disclosure Statement is appreciated.

Claims 1-20 stand rejected under 35 USC §103 as unpatentable over Horden (U.S. Patent 5,812,860, cited by the Applicant) in view of Shaffer (U.S. Patent 6,298,448). In the rejection of claims 1-20, the Examiner admits that "Horden et al do not teach a method of the circuits generating a signal indicative of their current operation" and "Horden et al fail to detail a method of the other circuits operable to output their current operation." These admissions are very much appreciated.

The Examiner speculates that "a routineer in the art would have been motivated to look for a teaching for the possible method of reducing the time required for switching performance levels of a processor," although the Examiner provides no reason why the lack of a teaching in Horden (of "a signal indicative of their current operation") would motivate one to try to find a method for "reducing the time required for switching performance levels of a processor." The Examiner has apparently omitted some portion of his rationale and, in view of the admission that Horden fails to teach "generating a signal indicative of their current operation," it is the

Examiner who must find this teaching in another prior art reference in order to combine those references under 35 USC §103.

In addition to a teaching of the generation of the specified "current operation signal" in another reference, it is also incumbent upon the Examiner to provide some "reason" or "motivation" for combining these two references.

It is noted that in order to clarify the distinctions over the prior art, Applicant has amended claims 1 and 11 to include the subject matter of claims 2 and 12 therein and has cancelled claims 2 and 12. Thus, not only does the cited combination of references have to generate a current operation signal ("responding to a change in said performance control signal"), but the current operation signal must be "indicative of a maximum power supply voltage that can currently be supported by said voltage controller."

With respect to former claim 2, in section 8 on page 8 of the Official Action, the Examiner alleges that Horden teaches "a voltage controller to generate a power signal for the processor at a plurality if [sic] different voltage levels [Col 4 lines 12-16]." Assuming the Examiner to be correct in his allegation, the Horden teaching of a voltage controller does not suggest "generating a current operation signal indicative of a maximum power supply voltage that can currently be supported by said voltage controller" and this is the teaching that is missing from both Horton and Shaffer.

Thus, even if the Examiner's statement is true that Horden teaches a "voltage controller" (formerly recited in claims 2 and 12 and now incorporated in independent claims 1 and 11), it does not teach the generation of "a signal indicative of their current operation."

In section 6 on page 3 of the outstanding Official Action, the Examiner concludes that the Shaffer reference teaches circuits which are "operable to inform the processor of its current output frequency, current operation [Col 3 lines 12-22]" in an apparent attempt to demonstrate where the teaching missing from Horton is disclosed in Shaffer. Looking at the cited portion of the Shaffer reference, it appears that the only information being passed to the CPU 20 along line 51 is the clock frequency and therefore control operation of the clock speed of CPU 20 ("clock module 50 is able to inform the CPU 20 of its output frequency through line 51, and the CPU 20 in turn can instruct through line 49 the clock module 50 to increase or decrease the output frequency as needed, thereby enabling the CPU 20 to regulate its own operating clock speed." Column 3, lines 14-19).

In Shaffer there is any indication of a direct correlation between a maximum power supply voltage that can currently be supported by a voltage controller and the clock speed feedback signal on line 51 as disclosed in Shaffer. The Examiner has failed to even allege where Shaffer contains any such teaching and, of course, such teaching would be necessary to establish a *prima facie* case of obviousness under 35 USC §103 in view of the admitted lack of such signal in the Horden reference.

Thus, Horden admittedly fails to teach generating a signal indicative of the circuit's operation and, in particular, where that signal is indicative of the maximum power supply voltage, and there is no allegation that Shaffer teaches any feedback indicative of "a maximum power supply voltage," although Shaffer does appear to teach a clock frequency feedback signal. Moreover, even if Horden teaches a voltage controller, it does not suggest that it teaches a voltage controller for generating a power signal at a plurality of different voltage levels and that

the current operation signal is indicative of a maximum power supply voltage that can currently be supported by said voltage controller. None of the claimed subject matter is disclosed or rendered obvious in the Horden reference and there is no allegation that it is disclosed or rendered obvious in the Shaffer reference. Therefore, the combination of claims 1 and 2 in amended claim 1 as well as the combination of claims 11 and 12 in amended claim 11 are clearly patentable over the Horden/Shaffer combination of references.

In addition to the failure to disclose the subject matter recited in Applicant's independent claims 1 and 11, the Examiner has provided no reason for one of ordinary skill in the art to combine the Horden and Shaffer references. The only discussion contained in the Official Action which could be construed as an attempt to provide a "reason" or "motivation" for combining the two references is contained in paragraph 7 on page 3. Here, the Examiner suggests that Horden and Shaffer are "analogous art," but merely being analogous art is insufficient support under the most recent Federal Circuit guidelines for combining references. The burden is on the Examiner to meet the Federal Circuit requirement that "the examiner [to] show a motivation to combine the references that create the case of obviousness." *In re Rouffet*, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1988). In explanation, the Federal Circuit has stated that

> the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *Id.*

In the present rationale, the Examiner merely suggests that Horden and Shaffer teach methods of controlling performance of a processor for power consumption purposes and broadly alleges that Shaffer covers the deficiencies of Horden by teaching "the detail of the other circuits operable to perform their current operation." (See page 3, section 7 of the outstanding Official Action).

Additionally, the Examiner's statement in paragraph 5, i.e., that "a routineer in the art would have been motivated to look for a teaching for the possible method of reducing the time required for switching performance levels of a processor" may be instructive. Even if the feedback signal on line 51 of Shaffer did provide a "current operation signal" as set out in Applicant's amended claims 1 and 11, providing such a signal to the Horden reference would not in itself reduce "switching time" by itself (some further techniques would be required and these are not shown in either document). Thus, it is clear that even if the two references were combined, they would not operate in the manner of Applicant's claimed invention.

In summary, neither Horden nor Shaffer disclose all of the structures and method steps set out in Applicant's independent claims 1 and 11 and claims dependent thereon. Additionally, the Examiner has failed to meet his burden of providing any "reason" or "motivation" for combining these two references. Finally, even if the references were combined, the alleged feedback for the purpose of "reducing the time required for switching performance levels of a processor" would not be accomplished by the alleged combination. Therefore, for any and all of the above reasons, the Horden/Shaffer combination simply does not disclose or render obvious independent claims 1 and 11 or claims dependent thereon and any further rejection thereunder is respectfully traversed.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1, 3-11 and 13-20 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicant's undersigned representative.

Respectfully submitted,

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